REMARKS

Claims 1-3, 5-12 and 15-23 are pending. Reconsideration of this application in light of the following remarks is respectfully requested.

The rejection of claims 1, 2, 5 to 11, 15 to 17, and 19 to 23 under 35 U.S.C. 103(a), as being unpatentable over United States Patent No. 5,481,563 (Hamre) in view of United States Patent No. 6,263,034 (Kanack et al), and the rejection of claims 3, 12 and 18 under 35 U.S.C. 103(a), as being unpatentable over Hamre in view of Kanack et al and United States Patent No. 6,100,724 (Yoshimura), are respectfully requested.

As applicant has previously discussed, the system disclosed in the Hamre reference uses two clock signals, i.e. a nominal clock and an early clock, both of which are derived from the data signal, and contain jitter (which may not matter in Hamre's system, since the results of the early clock are compared to those of the nominal clock). As a result, only a positive jitter peak can be established based on a statistical error rate performance of the early clock relative to the nominal clock.

The present invention eliminates the need for both the nominal and early clock signals, by counting the number of pulses from a single "offset", "jitter-free" reference clock signal that fall in each bit of the digital signal, and comparing that count to a predetermined number that would occur if there was no jitter. Then the number of times, when

the number of sampling times in any bit of the digital signal is different from the predetermined number, is counted and, from this count, the jitter is determined.

The clock signal according to the claimed invention is "offset" from the data signal; it is not just another clock signal, i.e. the delayed clock signal, as in the Hamre reference. In accordance with the claimed invention, the combination of offsetting and making the reference clock signal jitter free enable a single clock signal to provide: *occasions when the number of sampling times in any bit of said digital signal is different from the predetermined number,* whereby the number of occasions derived from the single reference clock signal are used to provide both low and high frequency jitter measurements.

Applicant's claimed invention is much simpler than the device disclosed in the Hamre reference, as it does not require the hardware to generate both the nominal and early clock signals, and enables the recovery of both a positive and negative peak by looking for any errors, not just statistical error rate information.

The device disclosed in the Kanack et al reference is designed to **reduce** jitter in an input signal by comparing a first clock signal, which is phase matched to the input signal, to a second "reduced jitter output clock", which naturally has reduced jitter, since it is independently generated by the VCO 48. The first clock signal disclosed in Kanack et al, i.e. the data sampling clock 66, ***"is used to adjust the frequency of VCO 48 allowing locking of VCO 48 to the frequency and phase of incoming input data signal 64."***

(col 4, lines 30 to 32). Accordingly, the first clock signal, which is based on, but not generated from, the input signal is not jitter free. The second clock signal, which is generated by the VCO 48 and the digital filter 42 is the "reduced jitter output clock". The results of the comparison are used to reduce the jitter in the original input signal.

It will be readily appreciated, therefore, that Kanack et al do not disclose or suggest generating a jitter free clock signal **from** the input data signal, and then using that jitter free clock signal to **measure** the jitter in the input data signal. As in the Hamre reference, Kanack et al require a pair of clock signals, as well as an independent clock generator to directly reduce the jitter in the input signal, not to measure the jitter using a jitter free clock signal generated from the original data signal.

Furthermore, there is no motivation to take the "reduced jitter output clock" from the Kanack et al reference and compare it to one of the clock signals or even the data signal in the Hamre et al reference, as both disclosures rely on a comparison of two clock signals. Applicant's claimed invention, on the other hand, totally eliminates the need for a second clock signal.

Neither prior art reference discloses or suggests the desire or the ability to eliminate one of the clock signals and the required signal generator by counting when the number of sampling times in any bit of the digital signal is different from a predetermined number. It is respectfully submitted, therefore, that a combination of two references, each disclosing the use of two independently generated clock

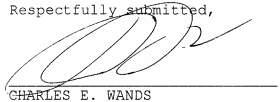
signals, will not result in the present invention, which requires only a single self-generated clock signal.

As such, it is respectfully submitted that all of the claims remaining in the application are in condition for allowance. Early and favorable consideration would be appreciated.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,



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